

APPLICATION FOR UNITED STATES LETTERS PATENT

INVENTORS: Jang Geun OH

TITLE: SYSTEM AND METHOD FOR OPTIMIZING CLOCK SPEED
GENERATION IN A COMPUTER

ATTORNEYS: FLESHNER & KIM, LLP
& P. O. Box 221200
ADDRESS: Chantilly, VA 20153-1200

DOCKET NO.: LT-0006

SYSTEM AND METHOD FOR OPTIMIZING CLOCK SPEED GENERATION IN A COMPUTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

[1] The present invention relates to an apparatus and a method of controlling clock frequency generation, and more particularly, to an apparatus and a method for a portable device.

2. Background of the Related Art

[1] In general, a portable device such as a notebook computer can be supplied with its necessary electric energy either by a battery or an AC power line. However, because battery capacity is limited, a notebook cannot be used for more than a few hours if its power is supplied from the battery.

[2] Fig. 1 is a simplified block diagram of a related art notebook. The notebook of Fig. 1 comprises a CPU 11 conducting ordinary well-known operations and functions; a bridge controller 12 conducting both assistant operations of the CPU 11 and management of memories, a video port, a bus, etc.; a video processor 13 for processing video data and outputting the processed data for video presentation; and a clock generator 10 providing a 100MHz clock signal 1 for the CPU 11 and the bridge controller 12, and a 66MHz clock signal 2 for the video processor 13.

[3] A PLL (Phase Lock Loop) circuit 110 is embedded in the CPU 11. The PLL circuit 110 multiplies the 100MHz clock from the clock generator 10 differently based on a current power supplying mode. For example, the PLL circuit 110 multiplies the 100MHz clock 1 by a factor of six to produce a 600MHz internal clock if an AC power mode (PWR mode) is detected, and it multiplies the 100MHz clock 1 by a factor of five to produce a 500MHz clock if a battery power mode is detected.

[4] Because power consumption of a CPU 11 is proportional to the speed of a clock driving the CPU 11, if a 500MHz internal clock is used in a battery supplying mode, processing speed is lowered and power dissipation is decreased in comparison with a 600MHz internal clock. Therefore, battery life is extended.

[5] However, in a related portable computer, a host bus 3 to which both a CPU 11 and a bridge controller 12 are connected is driven by a bus clock to bridge controller 12 whose speed is fixed regardless of power supplying mode. Therefore, power saving in a battery supplying mode is less effective.

[6] The above references are incorporated by reference herein where appropriate for appropriate teachings of additional or alternative details, features and/or technical background.

SUMMARY OF THE INVENTION

[7] An object of the invention is to solve at least the above problems and/or disadvantages and to provide at least the advantages described hereinafter.

[8] Another object of the present invention is to provide a method of reducing clock speed of a bus in order to extend battery suppliable time longer when electric energy is fed to a portable computer such as a notebook from an equipped battery.

[9] In order to achieve at least the above-described objects of the present invention in a whole or in part, there is provided a portable device having a CPU and a bridge controller operating in one of AC power mode or battery power mode, wherein the improvement includes a clock generator generating a first clock signal for the CPU and a second clock signal for the bridge controller, wherein first and second clock signals are two distinct clock signals outputted by the clock generator and have different frequencies.

[10] To further achieve at least the above-described objects of the present invention in a whole or in parts, there is provided a portable device having a CPU and a bridge controller, wherein the improvement includes a clock generator generating a first clock signal, and a clock adjustor operating in one of AC power mode or battery power mode, said clock adjustor generating a second clock signal for the CPU and a third clock signal for the bridge controller, wherein the second and third clock signals are two distinct clock signals outputted by the clock adjustor and have different frequencies.

10902154E0001

[11] To further achieve at least the above-described objects of the present invention in a whole or in parts, there is provided a method for optimizing clock speed generation, including receiving a base clock signal, multiplying the base clock signal by a first factor to produce a first higher frequency clock signal, wherein the first higher frequency clock signal is phase-locked with the base clock signal, receiving a power mode signal indicating either an AC or a battery source, and selectively outputting the first higher frequency clock signal to a first device when the AC source is indicated and outputting the base clock signal to the first device when the battery source is indicated.

[12] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[13] The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

[14] Fig. 1 is a partial block diagram of a related art computer;

[15] Fig. 2 is a partial block diagram of a portable computer in which a bus clock controlling apparatus in accordance with a preferred embodiment of the present invention is embedded;

[16] Fig. 3 is a detailed block diagram of the PLL circuit built in a controlling device according to the embodiment of Fig. 2;

[17] Fig. 4 is a block diagram of a portable computer in which another bus clock controlling apparatus in accordance with a preferred embodiment the present invention is embedded; and

[18] Fig. 5 is a detailed block diagram of the PLL block applying each clock to each device according to the embodiment of Fig. 4.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[19] In order that the invention may be fully understood, preferred embodiments thereof will now be described with reference to the accompanying drawings.

[20] Fig. 2 is a block diagram of a portable computer in which a bus clock controlling apparatus in accordance with the present invention is embedded. The portable computer of Fig. 2 includes a CPU 11, a bridge controller 22, and a video processor 23. The portable computer of Fig. 2 further comprises a clock generator 20 which may provide CPU 11, bridge controller 22 and video processor 23 with necessary clock signals.

[21] The clock generator 20 may provide the CPU 11 with a 100MHz CPU clock signals 101, the bridge controller 22 with a 66.7MHz host clock signals 102 (lower in frequency than the 100MHz CPU clock 101), and the video processor 23 with a 33.33MHz clock signal 103 (lower in frequency than a conventional 66MHz AGP clock).

[22] A PLL circuit 210 may be included in the CPU 11. As aforementioned, the PLL circuit 110 may multiply the 100MHz CPU clock 101 from the clock generator 20 selectively based on the current power supplying mode. For example, the PLL circuit 110 may multiply the frequency of a 100MHz clock 101 by six if an external AC power is fed, and it may multiply the frequency by five if a battery is supplying necessary electric energy.

[23] In addition, another PLL circuit 220 may be embedded in the bridge controller 22. The PLL circuit 220 may multiply the frequency of the 66.7MHz host clock 102 from the clock generator 20 by one and a half to produce a 100MHz PCI bus clock in an AC power supplying mode, and may use the 66.7MHz host clock 102 as it is without frequency multiplication in a battery supplying mode.

[24] Fig. 3 is a detailed block diagram of the PLL circuit 220. The PLL circuit 220 may include a phase comparator 221 outputting a DC voltage proportional to the phase difference between the 66.7MHz host clock 102 and a divided internal oscillating clock; a voltage controlled oscillator (VCO) 222 generating the internal oscillating clock of about 400MHz whose frequency varies in proportion to the level of the DC voltage

applied from the phase comparator 221; a 1/6 frequency divider 223 dividing the 400MHz internal oscillating clock by 6 to produce a 66.7MHz clock; a 1/4 frequency divider 224 dividing the 400MHz internal clock by 4 to produce a 100MHz clock; and a switch 225 selecting the inputted 66.7MHz host clock 102 or the divided 100MHz clock 102a in accordance with the power supplying mode to output a host bus clock or to use it as an internal operation clock.

[25] The PLL comparator 221 may output a DC signal to increase or decrease the frequency of the internal oscillating clock generated by VCO 222 in proportion to the phase difference between two applied signals, so that the two applied signals become in phase exactly. Therefore, the frequency of the internal oscillating clock may be six times as high as that of the inputted 66.7MHz host clock 102 while its phase is locked with the host clock 102. Accordingly, if the internal oscillating clock frequency is divided by 4, a 100MHz clock whose phase is locked with the inputted host clock 102 may be produced and it can be used as a bus clock of a host bus through the bridge controller 22.

[26] The switch 225 may select the 66.7MHz host clock 102 when the power supplying mode is indicative of the battery mode, while it may select the 100MHz clock 102a divided from the internal oscillating clock in the external AC supplying mode. If a battery is supplying electric energy, the above elements 221, 222, 223, and 224 need not be operative, thus it may be preferable to cut off power supply for them in that mode.

[27] The video processor 23 may also include PLL circuit 230. The PLL circuit 230 of the video processor 23 may multiply the 33.33MHz clock from the clock generator 20 by two to produce a 66.7MHz AGP video clock in AC power supplying mode, and may use the 33.33MHz clock without frequency multiplication in battery supplying mode.

[28] The structure of the PLL circuit 230 may be similar to that shown in Fig. 3 except for the frequency dividing ratio and other respects. In the PLL circuit 230 whose input frequency is 33.33MHz, a 200MHz-oscillating clock may be generated from an internal clock generator (corresponding to the element 222 of Fig. 3), and a 1/3 frequency divider (corresponding to the element 224 of Fig. 3) may be used. In this instance a clock output by the 1/3 frequency divider is at a frequency of 66.7MHz.

[29] In the portable computer configured as above, if a battery is supplying electric energy, the frequency of a bus clock provided to a host bus by the bridge controller 22 may be decreased to 66.7MHz from 100MHz, and the frequency of an internal clock used by the video processor 23 may also be decreased to 33.33MHz from 66.7MHz. This clock speed reduction results in extension of battery life.

[30] A detecting means, which outputs a signal indicating power supplying mode after detecting which power source between an external AC power and a battery is supplied at present, can be integrated into the bridge controller 22 or may be implemented as a separate device.

[31] Fig. 4 is a block diagram of a portable computer in which another bus clock controlling apparatus in accordance with the present invention is embedded. In the block diagram of Fig. 4, PLL circuits for reducing clock speed in battery mode may not be included in the bridge controller 32 and the video processor 33. Instead, a separate PLL block 40 may be included in the embodiment of Fig. 4. The PLL block 40, which can be manufactured with a customized semiconductor such as an ASIC (Application Specific Integrated Circuit), may provide each element with respective necessary clocks of mutually different frequency. A clock generator 30 may be further included in the embodiment of Fig. 4 to supply the PLL block 40 with a basic clock 114 of 33.33MHz.

[32] However, a PLL circuit 110 for producing 600MHz or 500MHz by multiplying 100MHz differently may be embedded in the CPU 11 as mentioned above.

[33] The frequency 33.33MHz of the basic clock 114 applied to the PLL block 40 from the clock generator 30 may be equal to the lowest among clock frequencies the PLL block 40 provides in battery supplying mode. The PLL block 40 may be configured as in Fig. 5 to supply all clocks, namely, 100MHz clock necessary to the CPU 11 regardless of power supplying mode, and 33.33MHz, 66.7MHz and 100MHz clocks which are selectively provided to the bridge controller 32 and video processor 33 according to power supplying mode.

[34] A phase comparator 421 of Fig. 5 may adjust the frequency of the approximately 200MHz oscillating clock of a VCO 422 in proportion to a detected phase

difference between the 33.33MHz clock 114 from clock generator 30 and a 1/6 divided clock from the 200MHz oscillating clock. As a result, the phase of the 200MHz oscillating clock may be locked with the applied 33.33MHz clock 114 from clock generator 30.

[35] In phase-locked state of the 200MHz clock, a 100MHz clock may be produced from a $\frac{1}{2}$ divider 423 dividing the 200MHz clock by two, and 66.7MHz clock may also be produced from a $\frac{1}{3}$ divider 425 dividing the 200MHz clock by three. Therefore, the 100MHz clock 111 from the $\frac{1}{2}$ divider 423 may be applied to the CPU 11 at all times.

[36] In the circuit of Fig. 5, switches 426a and 426b select 'A' terminals as input if power supplying mode is indicative of external AC, so that the 100MHz clock is applied to the bridge controller 32 as host clock 112 and the 66.7MHz clock is applied to the video processor 33 as AGP clock 113. If electric power is fed from a battery, 'B' terminals are chosen; therefore, the host clock 112 and the AGP clock 113 become 66.7MHz and 33.33MHz, respectively.

[37] Accordingly, lower frequency clocks in battery mode than in AC mode may be provided for corresponding devices, which means that power consumption is reduced when a battery is supplying necessary electric energy.

[38] In the embodiments of Figs. 2 and 4, the output clocks of the clock generators 20 and 30 may be applied without regard to power supplying mode.

Furthermore, in the embodiments of Figs. 2 and 4, clock frequency adjusting means may be embedded in the CPU, bridge controller, and video processors or implemented as a separate device.

[39] As can be appreciated, based on the disclosure of the preferred embodiments, the output of the clock generators 20 and 30 of Figs. 2 and 4, respectively, may be applied without raising the frequency during the battery power mode but increasing the clock frequency if an AC power mode is detected. Alternatively, the output of the clock generators 20 and 30 may be applied without frequency adjustment in the AC power mode but decreasing the clock frequency if a battery power mode is detected.

[40] In another embodiment, the clock frequency adjusting means may be integrated into a clock generator 30. The clock frequency adjusting means mentioned here is a device which adjusts or maintains frequency of an input clock based on which power source is feeding electric energy, and applies the frequency-adjusted or -maintained clock to external devices.

[41] An alternative embodiment of the invention, the frequency adjusting means may be embedded in other combinations of the clock generator, PLL ASIC, CPU, bridge controller, video processor, and/or other devices.

[42] The bus clock controlling apparatus of a portable computer according to the present invention reduces speed of a bus clock and a device clock in battery mode. Therefore, electric energy stored in a battery is saved, extending battery life.

[43] In addition, the present invention can be applied to a PCI bus for data communication among peripheral devices connected to the PCI bus by providing the clock to another Bridge controller for a PCI bus in the same way as for the host bus.

[44] The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.